Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.026”**

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**.026”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004” Min.**

**Backside Potential: Collector**

**Mask Ref: CP318V**

**APPROVED BY: DK DIE SIZE .026” X .026” DATE: 5/8/23**

**MFG: CENTRAL SEMI THICKNESS .007” P/N: 2N3501**

**DG 10.1.2**

#### Rev B, 7/1